Attention-Guided Hierarchical Feature Aggregation based FPGA Design for Low Delay Abnormal Detection System in Logistics

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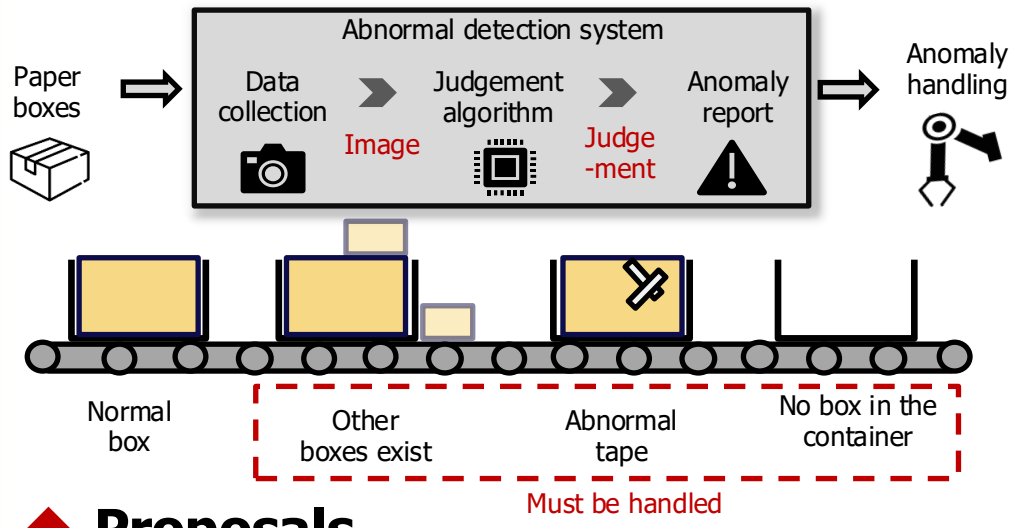
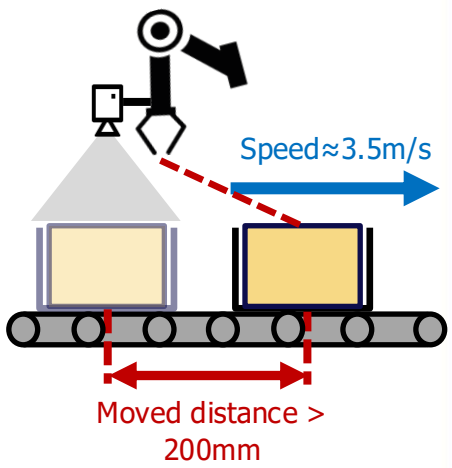
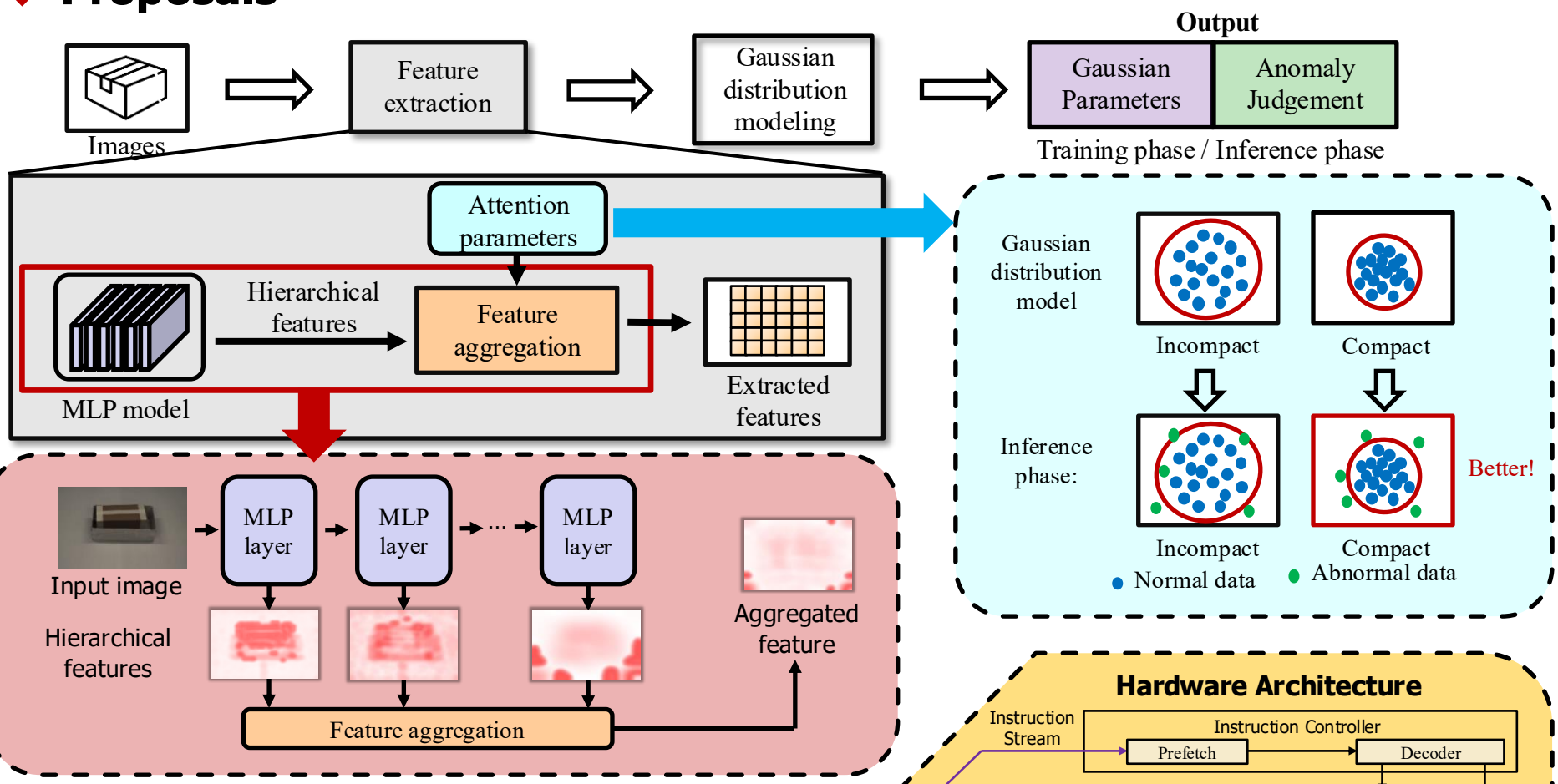
Background

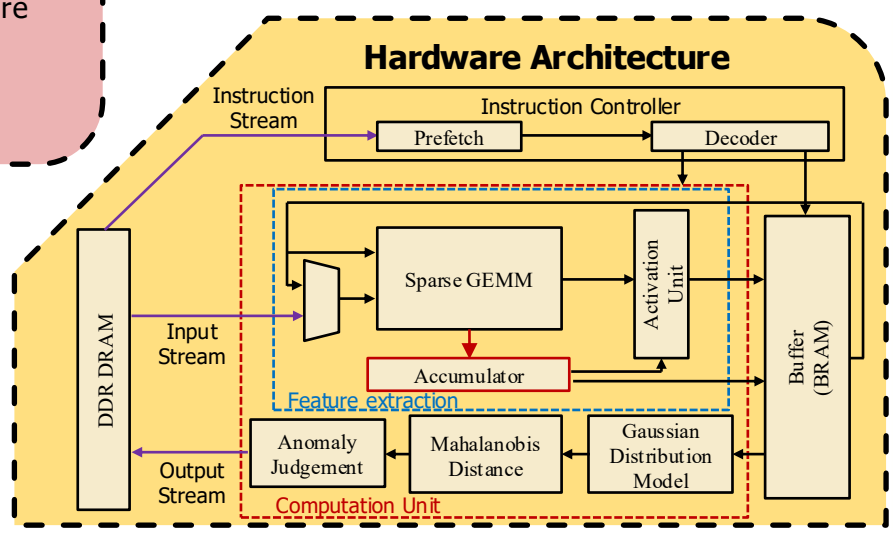


- Existing methods:
  - Implemented on high performance GPU
  - Focus on accuracy but long detection time
  - Conveyor belt must be slowed down or paused for anomaly handling



Proposals





Experiment Results

	Device	Precision ↑	Recall ↑	AUROC ↑
sMLP-T	GPU	0.9851	0.9975	0.9984
Baseline	GPU	0.9974	0.9657	0.9973
+P1	GPU	0.9962	0.9883	0.9991
Baseline	FPGA	0.9850	0.9348	0.9892
+P1	FPGA	0.9858	0.9849	0.9968
Zhang's	FPGA	0.9938	0.9018	0.9823
Wu's	GPU	0.9640	0.8890	0.9970
Gaus-AD	GPU	0.9947	0.8992	0.9851

Conclusion

- Improve the performance to 98.58% precision, 98.49% recall and 0.9968 AUROC on FPGA, reduce hardware design delay from 180.9 ms to 21.1 ms.

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